Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 24, with the following amended paragraph:

Global write data lines 126 and 128 are selectively coupled through N-channel transistors 120 and 122 respectively to local write data lines 116 and 118 in response to a write enable (WEN) signal applied to the gate terminals of transistors 120, 122. In turn, the local write data lines 116 and 118 are selectively coupled through N-channel transistors 110 and 112 respectively to complementary bit lines BL and BLB in response to a column write (YW) signal applied to the gate terminals of transistors 110 and 112 at line 114.

Please replace the paragraph beginning at page 7, line 3, with the following amended paragraph:

The column read amplifier power-gating circuit 200 comprises a number (e.g. 1088 in the embodiment shown, 64 of which are active) of conventional column read amplifiers 202 in conjunction with a large, separate power-gating N-channel transistor 206 which is controlled by a power-gating signal applied to its gate terminal on line 204. As will be more fully described hereinafter, the power-gating transistor 206 serves to couple or decouple the column read amplifier 202 to VSS in accordance with the signal placed on line 204 in consonance with other signals applied to the YR input.